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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,401	12/22/2003	Timothy J. Dupuis	SIL.P0068	7172

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EXAMINER	
NGUYEN, DUC M	

ART UNIT	PAPER NUMBER
2618	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/743,401	DUPUIS, TIMOTHY J.	
	Examiner	Art Unit	
	DUC M. NGUYEN	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 3-19, 21-40, 43-45* is/are pending in the application.

4a) Of the above claim(s) *7-13,15-19,22-29 and 31-40* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,14,18,21,30 and 43-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to applicant's response filed on 3/3/08. Claims 1, 3-19, 21-40, 43-45 are now pending in the present application. Claims 7-13, 15-19, 22-29, 31-40 are withdrawn from consideration.

Claim Rejections - 35 USC ∋ 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims **1, 3-4, 14, 18, 30, 43-45** are rejected under 35 U.S.C. 103(a) as being unpatentable by **Blake et al** (US **6,847,904**) in view of **Tomasz** (US **6,400,416**) and **Amar** et al (US **5,886,658**).

Regarding claim **1**, **Blake** discloses an RF amplifier formed using an integrated circuit (see Fig. 1 and Abstract), comprising

- A amplifier (see Fig. 1) and
- A serial interface formed using the integrated circuit for sending and receiving signal (see Fig. 1 and col. 5, line 25 – col. 6, line 7).

Although **Blake** does not specifically disclose the PGA amplifier is the power amplifier, one skilled in the art would recognize that a power amplifier would work equally well with Blake's teaching regarding serial interface formed using the integrated circuit. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to apply Blake's teaching to a power amplifier, for utilizing advantages of the serial interface such minimizing pin count of the IC package (see col. 5, lines 55-60). Therefore, the claimed limitation regarding the power amplifier is made obvious by Blake.

Further, since **Blake** teaches a gain selection switches 110 to control the operation of the amplifier, one skilled in the art would recognize that the gain selection switches would select/switch a gain adjust either via a serial bus (i.e, SDI input) or via the external input (Vref, see col. 6, lines 19-23) in the similar way as suggested by **Tomasz** (see Fig. 5 and col. 6, lines 32-42 regarding amplifier adjust via external pin or serial bus). Note that the chip select CS pin for controlling functions of the SPI (see **Blake**, col. 5, line 55 – col. 6, lines 7) would act as the serial bus control pin when the CS is at logic low level (i.e, enable SDI input) and would disable the serial bus (i.e, disable SDI input) when the CS is at the logic high level in the similar way as disclosed by **Amar** (see Fig. 4). Therefore, with the broadest reasonable interpretation, the chip select CS pin would read on the claimed "mode control pin" for selecting a serial interface mode (SDI/SPI enable) or the non-serial interface mode (SDI disable and the gain would be controlled/selected based on the Vref value). Therefore, claimed limitations are made obvious by Blake in view of Tomasz and Amar.

In an alternative way, **Tomasz** would obviously teach all the claimed limitations (see Fig. 5, col. 6, lines 32-42) except for explicitly teach a mode control pin and a power amplifier. However, by utilizing a chip select CS pin for a 3-wire serial bus as suggested by **Blake** (see Fig. 2) and **Amar** (see Fig. 4), the chip select CS pin would act as the serial bus control pin when the CS is at logic low level (enable SDI input) and would disable the serial bus (disable SDI input) when the CS is at the high level, the CS pin would read on the claimed "mode control pin" for selecting a serial interface mode (SDI enable) or the non-serial interface mode (SDI disable) for controlling the gain adjusted via either the serial bus or the external pin as suggested by **Tomasz** in col. 6, lines 32-42. Therefore, **Tomasz** would obviously suggest the claimed "mode control pin" in order to adjust the amplifier gain via either the serial bus or the dedicated external pin by utilizing a 3-wire bus. Further, it would have been obvious to one skilled in the art at the time the invention was made to modify Tomasz's teaching to a power amplifier as well because it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations *Ex parte Masham* 2 USPQ2d 1647 1987).

Regarding claims **3-4**, the claims are rejected the same reason as set forth in claim 1 above. In addition, **Blake**, in view of **Tomasz**, as modified would teach a second interface pin as claimed, in order to achieve various control functions for the amplifier either via the external pin or via the serial bus pins (see Tomasz, col. 6, lines 32-42).

Regarding claim **14,** the claim is rejected the same reason as set forth in claim 4 above. In addition, since one skilled in the art would recognize that the amplifier circuit as disclosed by Blake would applicable to a wireless transceiver and would work equally well, it would have been obvious to one skilled in the art at the time the invention was made to further modify Blake for providing a transceiver coupled a serial bus as claimed, for utilizing advantages of the serial interface in Blake such as minimizing pin count of the IC package (see col. 5, lines 55-60) for controlling the transceiver.

Regarding claim **18,** the claim is rejected the same reason as set forth in claim 14 above. In addition, since **Blake** teaches the serial interface is used control the function of the amplifier such as gains, bandwidth, power consumption, input offset correction, frequency response, etc, (see col. 2, lines 23-42 and Fig. 1), it is clear that Blake as modified would obviously teach a band control signal utilizing the serial bus as claimed, in order to select a band based on the band control signal (see Fig. 1 regarding MUX 104).

Regarding claim **30,** the claim is rejected the same reason as set forth in claim 1 above. In addition, since using a baseband controller to adjust the gain of the power amplifier is well known in the art, it would have been obvious to one skilled in the art at the time the invention was made to further modify Blake for providing a baseband controller as claimed, in order to control the output gain of the power amplifier.

Regarding claim **43,** the claim is rejected the same reason as set forth in claim 3 above.

Regarding claim **44**, the claim is rejected the same reason as set forth in claim 4 above.

Regarding claim **45**, the claim is rejected the same reason as set forth in claim 30 above. In addition, since **Blake** teaches the serial interface is used control the function of the amplifier such as gains, bandwidth, power consumption, input offset correction, frequency response, etc, (see col. 2, lines 23-42 and Fig. 1), it is clear that Blake as modified would obviously teach a band control signal utilizing the serial bus as claimed, in order to select a band based on the band control signal (see Fig. 1 regarding MUX 104).

3. Claims **5-6** are rejected under 35 U.S.C. 103(a) as being unpatentable by **Blake** in view of **Tomasz** and **Amar** and further in view of **Richard et al** (US **6,894, 266**).

Regarding claim **5**, the claim is rejected the same reason as set forth in claim 1 above. In addition, since the IC package in Blake would require a power supply to operate, it would have been obvious to one skilled in the art at the time the invention was made to provide the internal voltage source via a control pin as disclosed by **Richard** (see col. 5, lines 32-37 and col. 6, lines 20-35), in order to provide the supply voltage for registers of the IC package while minimizing the number of pins for the IC packages.

Regarding claim **6**, the claim is rejected the same reason as set forth in claim 5 above. In addition, **Richard** discloses the pin is used to supply power in the serial-in fashion only (see col. 5, lines 37-38).

4. Claims **5-6, 21** are rejected under 35 U.S.C. 103(a) as being unpatentable by **Blake** in view of **Tomasz** and **Amar** and further in view of **Collins et al** (US **5,724,009**).

Regarding claim **5**, the claim is rejected the same reason as set forth in claim 1 above. In addition, since the IC package in Blake would require a power supply to operate, it would have been obvious to one skilled in the art at the time the invention was made to provide the internal voltage source via a control pin as disclosed by **Collins** (see col. 2, line 58 – col. 3, line 7), in order to provide the supply voltage for digital circuitry (registers) of the IC package while minimizing the number of pins for the IC packages.

Regarding claim **6**, the claim is rejected the same reason as set forth in claim 5 above. In addition, since the supply voltage is used for operating the digital circuitry, it is clear that it is used as internal voltage source only for serial data input.

Regarding claim **21**, the claim is rejected the same reason as set forth in claim 5 above.

Response to Arguments

5. Applicant's arguments with respect to claims 1, 14, 30 have been considered but are moot in view of the new ground(s) of rejection.

6. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(571) 273-8300 (for **formal** communications intended for entry)

(571)-273-7893 (for informal or **draft** communications).

Hand-delivered responses should be brought to Customer Service Window, Randolph Building, 401 Dulany Street, Alexandria, VA 22314.

Any inquiry concerning this communication or communications from the examiner should be directed to Duc M. Nguyen whose telephone number is (571) 272-7893, Monday-Thursday (9:00 AM - 5:00 PM).

Or to Nay Maung (Supervisor) whose telephone number is (571) 272-7882.

/Duc M. Nguyen/

Primary Examiner, Art Unit 2618

June 1, 2008